

Lecture #23

Warning for HW Assignments and Exams:

- Make sure your writing is legible !!

OUTLINE

- MOSFET I_D vs. V_{GS} characteristic
- Circuit models for the MOSFET
 - resistive switch model
 - small-signal model

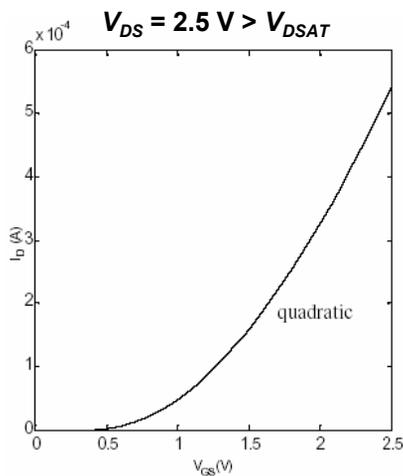
Reference Reading

- Rabaey *et al.*: Chapter 3.3.2
- Howe & Sodini: Chapter 4.5

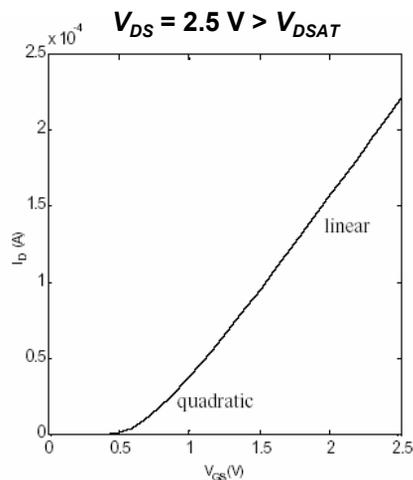
MOSFET I_D vs. V_{GS} Characteristic

- Typically, V_{DS} is fixed when I_D is plotted as a function of V_{GS}

Long-channel MOSFET

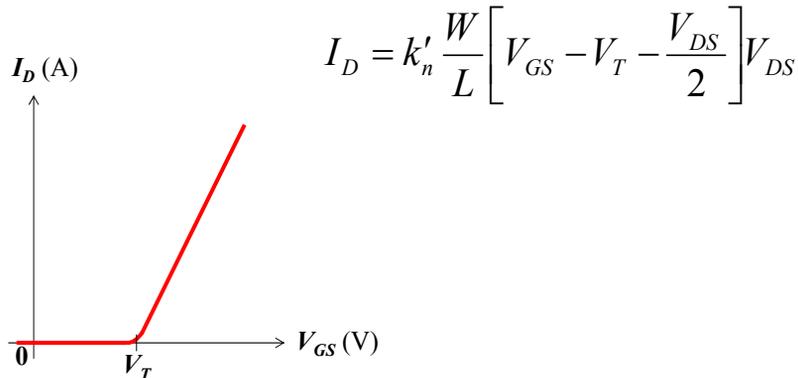


Short-channel MOSFET



MOSFET V_T Measurement

- V_T can be determined by plotting I_D vs. V_{GS} , using a low value of V_{DS} :



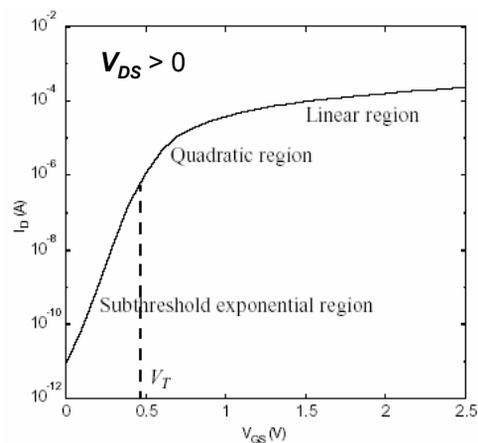
Subthreshold Conduction (Leakage Current)

- The transition from the ON state to the OFF state is gradual. This can be seen more clearly when I_D is plotted on a logarithmic scale:

- In the subthreshold ($V_{GS} < V_T$) region,

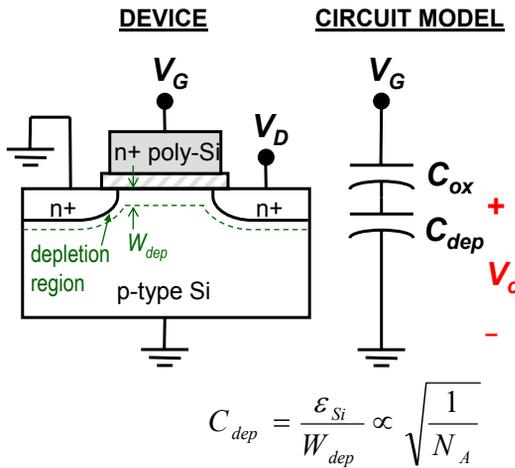
$$I_D \propto \exp\left(\frac{qV_{GS}}{nkT}\right)$$

This is essentially the channel-source pn junction current. (Some electrons diffuse from the source into the channel, if this pn junction is forward biased.)



Qualitative Explanation for Subthreshold Leakage

- The channel V_c (at the Si surface) is capacitively coupled to the gate voltage V_G :



Using the capacitive voltage divider formula (Lecture 12, Slide 7):

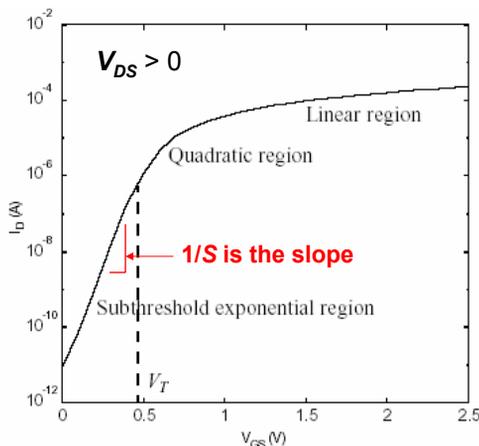
$$\Delta V_c = \frac{C_{ox}}{C_{ox} + C_{dep}} \Delta V_G$$

The forward bias on the channel-source pn junction increases with V_G scaled by the factor $C_{ox} / (C_{ox} + C_{dep})$

$$\Rightarrow n = \frac{C_{ox} + C_{dep}}{C_{ox}} = 1 + \frac{C_{dep}}{C_{ox}}$$

Slope Factor (or Subthreshold Swing) S

- S is defined to be the inverse slope of the $\log(I_D)$ vs. V_{GS} characteristic in the subthreshold region:



$$S \equiv n \left(\frac{kT}{q} \right) \ln(10)$$

Units: Volts per decade

Note that $S \geq 60$ mV/dec at room temperature:

$$\left(\frac{kT}{q} \right) \ln(10) = 60 \text{ mV}$$

V_T Design Trade-Off

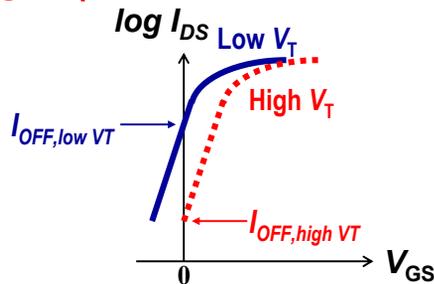
(Important consideration for digital-circuit applications)

- Low V_T is desirable for high ON current

$$I_{DSAT} \propto (V_{DD} - V_T)^\eta \quad 1 < \eta < 2$$

where V_{DD} is the power-supply voltage

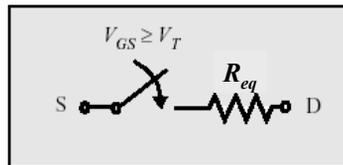
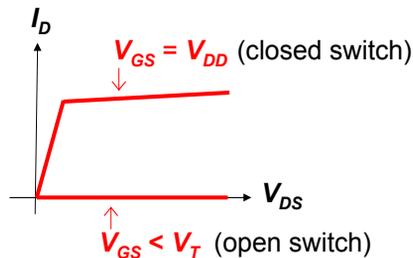
...but high V_T is needed for low OFF current



The MOSFET as a Resistive Switch

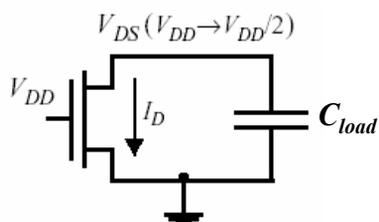
- For digital circuit applications, the MOSFET is either OFF ($V_{GS} < V_T$) or ON ($V_{GS} = V_{DD}$). Thus, we only need to consider two I_D vs. V_{DS} curves:

1. the curve for $V_{GS} < V_T$
2. the curve for $V_{GS} = V_{DD}$



Equivalent Resistance R_{eq}

- In a digital circuit, an n-channel MOSFET in the ON state is typically used to discharge a capacitor connected to its drain terminal:
 - gate voltage $V_G = V_{DD}$
 - source voltage $V_S = 0$ V
 - drain voltage V_D initially at V_{DD} , discharging toward 0 V



The value of R_{eq} should be set to the value which gives the correct propagation delay (time required for output to fall to $\frac{1}{2}V_{DD}$):

$$I_{DSATn} = \frac{k'_n W}{2 L} (V_{DD} - V_{Tn})^2 \longrightarrow R_{eq} \cong \frac{3}{4} \frac{V_{DD}}{I_{DSATn}} \left(1 - \frac{5}{6} \lambda_n V_{DD} \right)$$

Typical MOSFET Parameter Values

- For a given MOSFET fabrication process technology, the following parameters are known:
 - V_T (~ 0.5 V)
 - C_{ox} and k' (< 0.001 A/V²)
 - V_{DSAT} (≤ 1 V)
 - λ (≤ 0.1 V⁻¹)

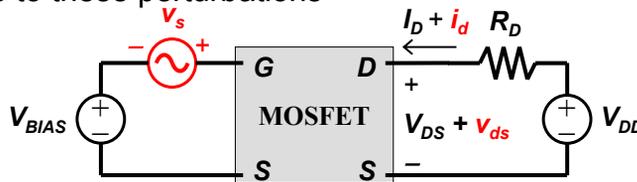
Example R_{eq} values for 0.25 μ m technology ($W = L$):

V_{DD} (V)	1	1.5	2	2.5
NMOS (k Ω)	35	19	15	13
PMOS (k Ω)	115	55	38	31

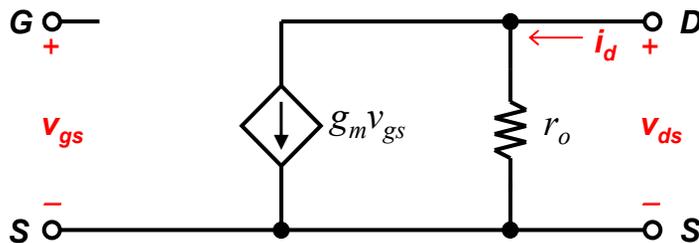
How can R_{eq} be decreased?

MOSFET Model for Analog Circuits

- For analog circuit applications, the MOSFET is biased in the saturation region, and the circuit is designed to process incremental signals.
 - A **DC operating point** is established by the **bias voltages** V_{BIAS} and V_{DD} , such that $V_{DS} > V_{GS} - V_T$
 - Incremental voltages v_s and v_{ds} that are much smaller in magnitude perturb the operating point
 - The MOSFET **small-signal model** is a circuit which models the change in the drain current (i_d) in response to these perturbations



NMOSFET Small-Signal Model



$$i_d = \frac{\partial i_D}{\partial v_{GS}} v_{gs} + \frac{\partial i_D}{\partial v_{DS}} v_{ds} = g_m v_{gs} + g_o v_{ds}$$

$$g_m \equiv \frac{\partial i_D}{\partial v_{GS}} \cong \frac{W}{L} k' (V_{GS} - V_T) \quad \text{transconductance}$$

$$g_o \equiv \frac{\partial i_D}{\partial v_{DS}} \cong \lambda I_D \quad \text{output conductance}$$