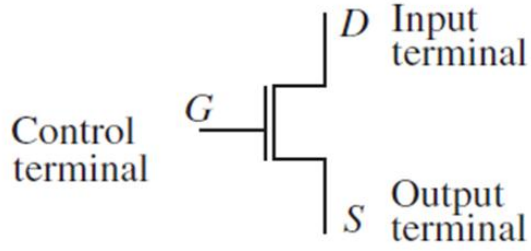
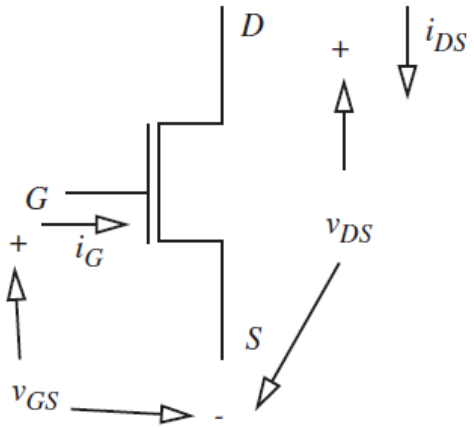
MOSFET Handout

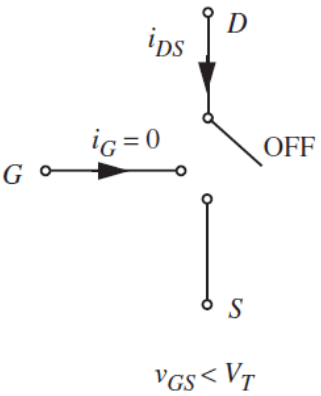
MOSFETs are three terminal devices where the control terminal or "gate" effectively controls the connectivity of the drain (D) and source (S) terminals. Below, on the left, we have a drawing of a MOSFET as it will appear in our circuits. On the right, we have various current and voltage definitions that we will be interested in finding.

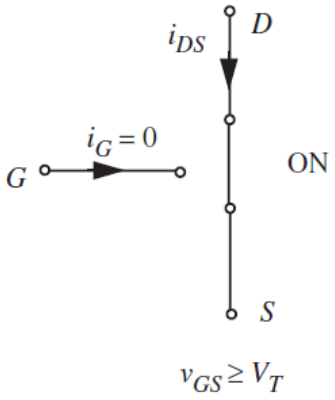




S Model

We have several models for the MOSFET. The first is the simplest, which the book calls the "S Model". In this case, the MOSFET is modeled as an ideal switch with behavior as shown below:



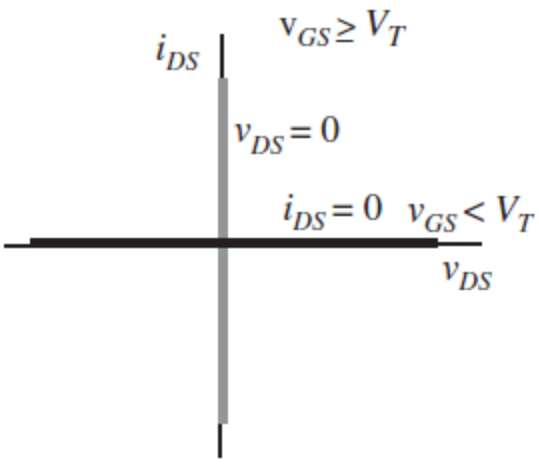


Or algebraically, we represent this as:

$$i_{DS} = 0 \text{ if } V_{GS} < V_T$$

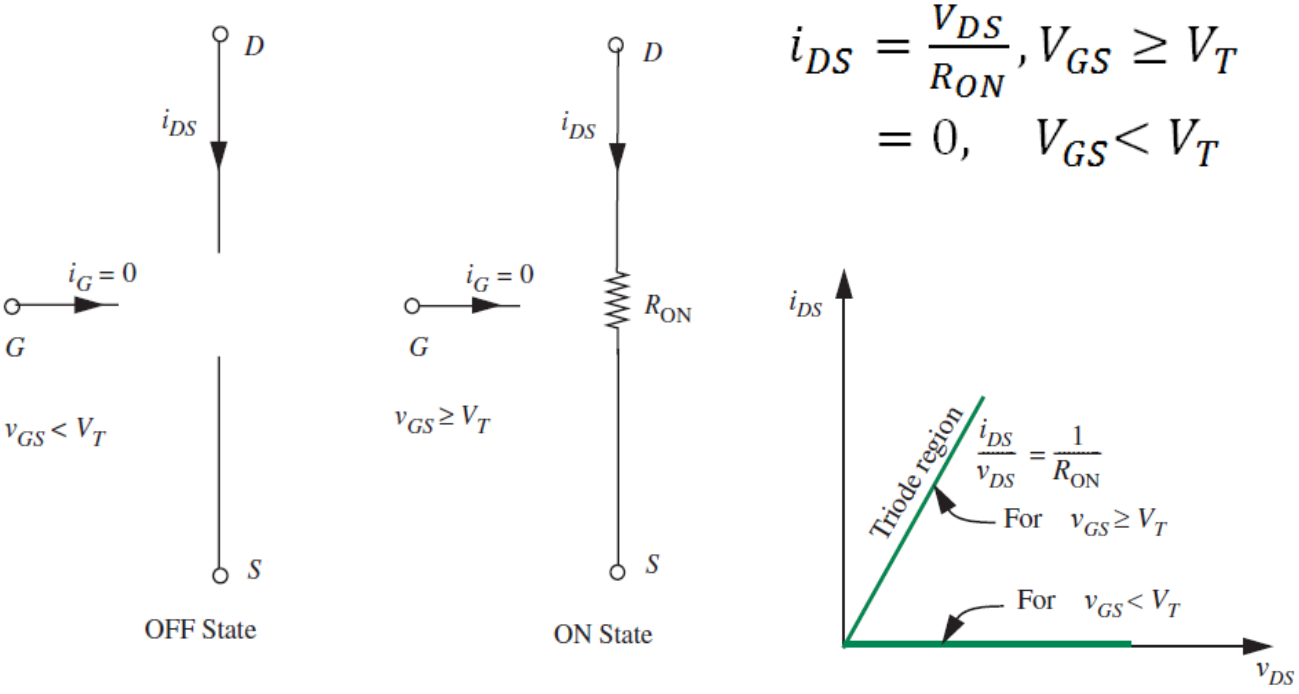
$$V_{DS} = 0 \text{ if } V_{GS} \geq V_T$$

Or as a $i_{DS} - v_{DS}$ characteristic, we can represent the MOSFET as shown on the back:



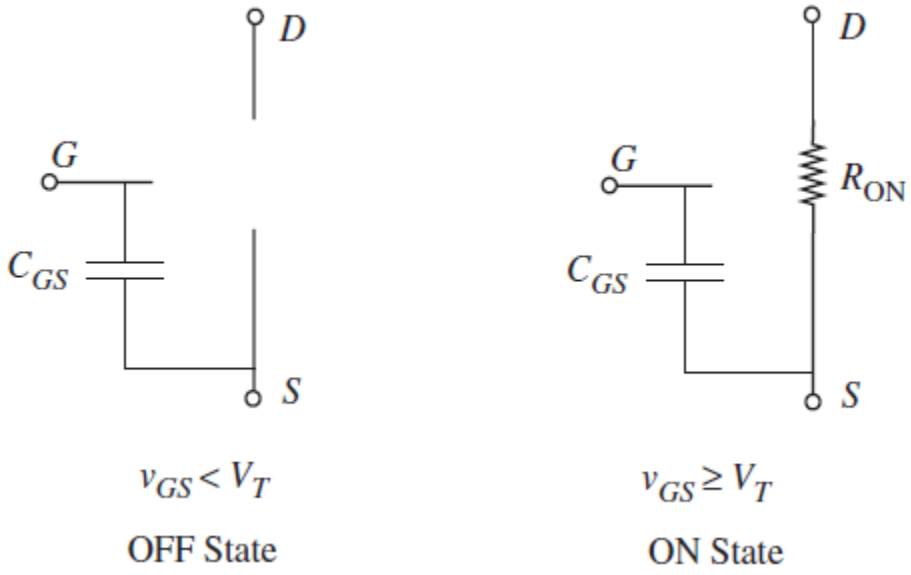
SR Model

Real MOSFETs have an effective resistance when on. In the SR model, we include the resistance of the MOSFET. This is still a crude approximation, but it is much more realistic than the S model. The model is summarized below:

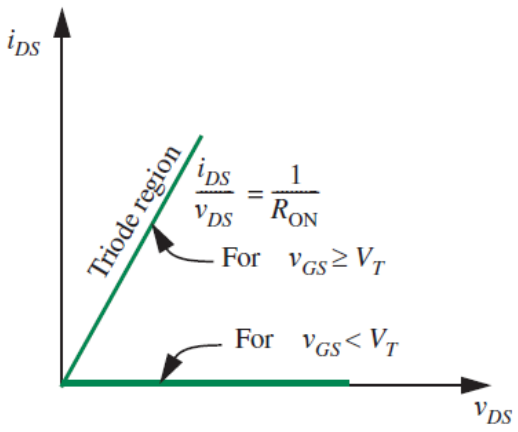


SRC Model

Finally, we have SRC Model of the MOSFET, which includes the capacitance of the gate. This will be necessary if we want to model the time it takes for a gate to switch. The SRC model is given as shown below:



Our algebraic equation and $i_{DS} - V_{DS}$ characteristic is still the same as in our SR model, but now V_{GS} is the voltage of a capacitor and will take time to increase when something tries driving it.



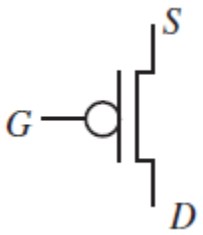
$$i_{DS} = \frac{V_{DS}}{R_{ON}}, V_{GS} \geq V_T$$
$$= 0, \quad V_{GS} < V_T$$

Note that gate current is now no longer zero, and is given by the equation. This equation for gate current will be the heart of our dynamic power calculations:

$$i_G = C_{GS}\frac{dv_{GS}}{dt}$$

PMOS Transistors

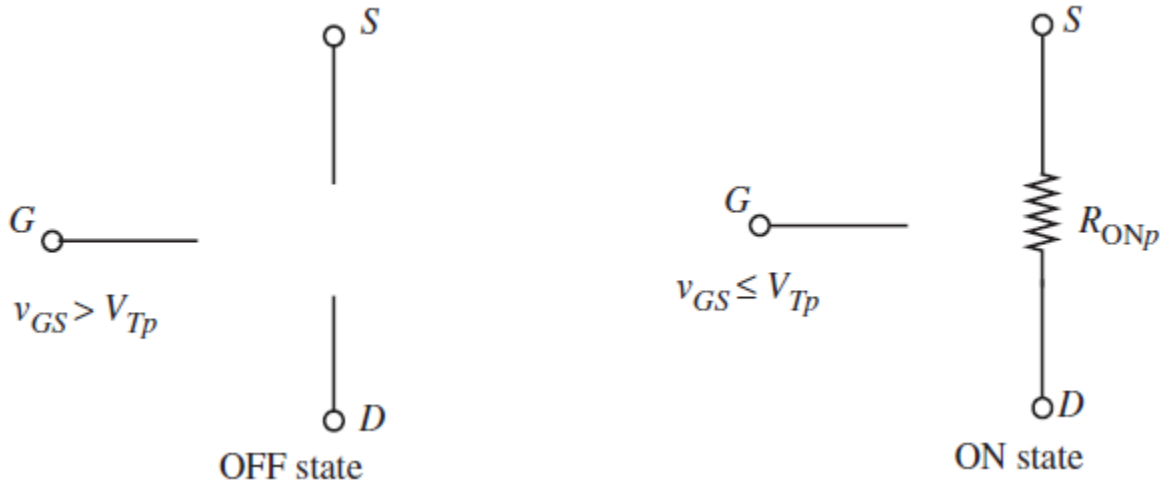
PMOS transistors are almost identical in function to NMOS transistors. They are given by the following schematic symbol:



Note that we usually draw our PMOS transistors with source (S) on top!

The difference between a PMOS and NMOS is that the voltage V_{GS} must be LESS than the threshold voltage in order to be on. Accordingly, the threshold voltages that we'll typically use will be small or negative voltages.

The SR Model of a PMOS transistor, for example, is:



Or algebraically:

$$i_{DS} = \frac{V_{DS}}{R_{ONp}}, V_{GS} \leq V_T$$
$$= 0, \quad V_{GS} > V_T$$